Code No: 9A10504/R09

B.Tech. III Year II Semester Regular & Supplementary Examinations

Set-4

April/May - 2013

LINEAR AND DIGITAL IC APPLICATIONS

(Common to EEE and MCT)

Time: 3 Hours | Max. Marks: 70

*Answer any **FIVE** Questions*

*All Questions carry **Equal** Marks*

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1. (a) Explain how large open circuit voltage gain of an op-amp can be obtained by using cascading of differential amplifier stages.

   (b) Explain the function of various blocks in block diagram of an op-amp.

2. (a) With suitable circuit diagram explain the operation of a triangular wave generator using a comparator and a integrator.

   (b) What is an instrumentation amplifier? List any three applications of the instrumentation amplifier.

3. (a) Explain frequency translation and FM detection applications of PLL.

   (b) Derive an expression for capture range of PLL.

4. (a) Draw the circuit for CMOS OR logic gate and explain its working clearly.

   (b) Which CMOS or TTL logic family has the strongest output driving capability? Explain.

5. (a) Explain how CMOS-TTL interfacing can be achieved. Give the input and output levels of voltages, explain briefly.

   (b) Explain low voltage CMOS logic and ECL.

6. (a) Design the logic circuit and write a data - flow style VHDL program for the following function:

   $F(X) = \Sigma A, B, C, D (1, 4, 5, 7, 12, 14, 15) + d (3, 11)$.

   (b) Explain the use of packages. Give the syntax and structure of a package in VHDL.

7. (a) Write VHDL program for 8-bit comparator circuit. Using this entity write VHDL program for 24-bit comparator.

   (b) Design a 4-bit carry look ahead adder using gates.

8. (a) Explain with neat sketch how four bits 1110 are serially entered into the shift register.(b) With neat circuit diagram explain a master-slave flip-flop and also draw the timing diagram.